

**B TECH  
(SEM IV) THEORY EXAMINATION 2017-18  
COMPUTER ARCHITECTURE AND ORGANIZATION**

*Time: 3 Hours**Total Marks: 100*

**Note:** 1. Attempt all Sections. If require any missing data; then choose suitably.

**SECTION A**

**1. Attempt all questions in brief. 2 x 10 = 20**

- a) Discuss the advantages and disadvantages of PLD's.
- b) Explain the Design Methodology and the Design Process.
- c) What are Combinational Array Multipliers?
- d) What do you understand by the data path and data path design?
- e) Explain Micro-operation & Microinstruction.
- f) What do you mean by fixed point arithmetic?
- g) Discuss the basic concepts of Control Design.
- h) Describe a CPU control unit.
- i) Describe the various Communication methods.
- j) Define VHDL. State the features and applications of VHDL.

**SECTION B**

**2. Attempt any three of the following: 10 x 3 = 30**

- a) Design a Register level 4-bit magnitude comparator and describe its operation..
- b) What are the components at processor design level in a computer system? Discuss various design issues at processor level.
- c) What do you mean by the structure and behavior of a system? Give the behavioral VHDL description .of half adder.
- d) Define a micro-program sequencer. Draw the micro programmed CPU employing a micro-program sequencer. Write a short note on multiplier control unit
- e) Differentiate between Address translation and Memory allocation in relation to memory organization. Also describe the multiplier control unit.

**SECTION C**

**3. Attempt any one part of the following: 10 x 1 = 10**

- (a) Design a 4-bit stream serial adder. Draw and explain the block diagram with truth table.
- (b) Explain the Register level design. Describe the major component types at the register level. Describe any register level component in detail.

**4. Attempt any one part of the following: 10 x 1 = 10**

- (a) Differentiate between RISC and CISC based microprocessors. Describe the RISC based instruction format.
- (b) Give the overview of CPU behavior using a flowchart. Also draw the block diagram for processor memory communication with and without cache.

5. Attempt any *one* part of the following: **10 x 1 = 10**

- (a) Explain how Booth's algorithm is suitable for signed number multiplication. Perform the multiplication of following using Booth algorithm ( $-4 \times -5$ ).
- (b) Write a program to evaluate the arithmetic statement  $X = (A+B) \times (C \times D)$ . Use an accumulator type computer with one address instruction.

6. Attempt any *one* part of the following: **10 x 1 = 10**

- (a) Explain the different types of pipelining. Also write a short note on performance and hazards of pipelining.
- (b) Differentiate between hardwired control & Micro programmed control. Explain each method in detail.

7. Attempt any *one* part of the following: **10 x 1 = 10**

- (a) Explain the Memory organization. Describe the Multi level memories.
- (b) Discuss the various types of address mapping used in cache memory. Give a comparison of the structure Vs performance.