Printed Pages: 3 **EEC 034**

(Following Paper ID and Roll No. to be filled in your Answer Books)	
Paper ID : 131854	**Roll No.**

B.TECH.

Theory Examination (Semester-VIII) 2015-16

INTEGRATED CIRCUIT TECHNOLOGY
(VLSI TECHNOLOGY)

Time : 3 Hours ***Max. Marks : 100***

Section-A

1. Attempt all questions. All questions carry equal marks (10×2 = 20)

(a) What is Epitaxial Growth? Give its types.

(b) What is diffusion? Define in reference with ICT.

(c) Give the name of material with the chemical formula which is used for the deposition of Polysilicon.

(d) Define nuclear stopping and electronic stopping.

(e) What is oxidation? What is the impact of presence of water while oxidation?

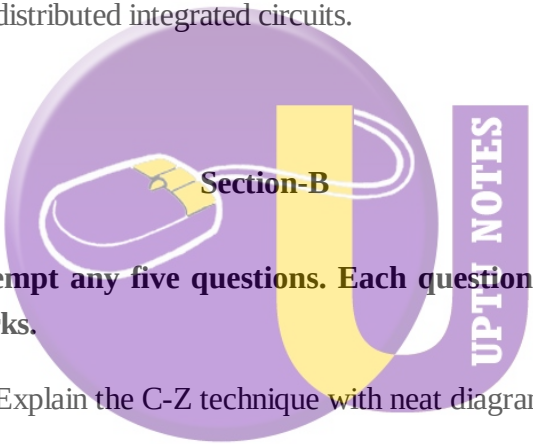
(f) What is Etching? Define Wet etching.

(g) What is Film Deposition? Also define the metallization.

(h) Define Lithography and photolithography.

(i) Give the name of two different types of IC packages. Define them on the basis of material used.

(j) List the advantages of Monolithic Integrated circuit over distributed integrated circuits.



Section-B

2. Attempt any five questions. Each question carries 10 marks. [5×10=50]

(a) Explain the C-Z technique with neat diagram.

(b) What are the major package design considerations for IC designing?

(c) What do you mean by silicon on insulator? Explain in details about SOI,SOS and Silicon on amorphous material

(d) What is molecular beam Epitaxy? Explain with neat diagram.

(e) Discuss all four types of deposition reactors with advantages and disadvantages.

(f) What is Ion implantation? Describe about the range theory of Ion implantation.

(g) Explain the fabrication sequence on Bipolar Junction Technology.

Section-C

Attempt any two questions. Each question carries 15 marks. (2×15=30)

3. Derive the Fick's one dimensional diffusion equation. And detail about the constant diffusivity and concentration, temperature dependency of diffusivity in terms of Fick's Equation.

4. Give the fabrication sequence of CMOS IC Technology. Also provide the information of different design considerations while CMOS IC fabrication in detail.

5. What is EGS? Discuss different steps in preparing wafers from raw silicon. Also detail about the Silicon Shaping.