Printed Pages: 4 **NEC-012**

(Following Paper ID and Roll No. to be filled in your Answer Books)	
Paper ID : 131662	**Roll No.**

B.TECH

Theory Examination (Semester-VI) 2015-16

COMPUTER ARCHITECTURE & ORGANIZATION

Time : 3 Hours ***Max. Marks : 100***

Section-A

1. Attempt all parts. All parts carry equal marks. Write answer of each part in sort. (2×10 = 20)

(a) Find 2's complement of $(11011100)_2$.

(b) Give any three examples of embedded processor chips.

(c) What do you mean by interrupt?

(d) Draw the block diagram of a computer system.

(e) Discuss the various hazards that might arise in a pipeline.

(f) What is Multiprogramming & Pipelining?

(g) What do you mean by effective address of data.

(h) What is Address Mapping?

(i) Write down the general formulas for floating-point operations.

(j) What is the need of Cache memory?

Section-B

2. Attempt any five questions from this section. (10×5 = 50)

(a) What is DMA? Explain DMA operation with a suitable diagram.

(b) Draw and explain virtual memory organization.

(c) Discuss various classifications of parallel processing mechanisms in uniprocessor Computers. Also discuss why array computers are termed as parallel computers?

(d) Design a 4-bit Carry-Look ahead Adder and explain its operation with an example.

(e) List various OS types and explain any one of them.

(f) What do you mean by design methodology? Write a short note on register level components.

(g) What is DMA? Why DMA is preferred over other mehtods for transferring data between expansion cards and computer memory?

(h) Describe CPU organization in detail along with features.

Section-C

Note : Attempt any two questions in this section. (15×2 = 30)

3. Define Booth's algorithm. Is it possible to design signed number Multiplication by using Booth's algorithm? Draw a flowchart and perform multiplication for signed number.

4. Write a short note on the following :

(a) PLD

(b) Programmed I/O

(c) Bus Structure

5. What are different types of pipelining? Explain each of them thoroughly. Also write a short note on performance and hazard of pipelining.

OR

What is Cache Memory? How is it implemented? A two way set associated cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K x32.

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of cache memory?