Printed Pages: 3 **NEN-021**

(Following Paper ID and Roll No. to be filled in your Answer Books)	
Paper ID :121666	**Roll No.**

B. TECH.

Theory Examination (Semester-VI) 2015-16

VLSI DESIGN

Time : 3 Hours ***Max. Marks : 100***

Section-A

1. Attempt all Questions. All Questions carry equal marks. Write answer of each in short. (2×10=20)

(a) List the advantages of SOI CMOS process

(b) Distinguish electrically alterable and non-electrically alterable ROM.

(c) Compare nMOS and pMOS devices.

(d) Give idea on enhancement and depletion mode devices.

(e) Comment on continuous assignment statement in Verilog HDL.

(f) What is a task in Verilog?

(g) Give the application of PLA.

(h) Define transmission gate.

(i) Define the aim of Adhoe test technique.

(j) State difference between functionality test and manufacturing test.

Section-B

2. Attempt any five questions from this section.. **(10×5=50)**

(a) Draw and explain the n-well process.

(b) Explain the twin tub process with a neat diagram.

(c) Discuss the origin of latch up problems in CMOS circuits with necessary diagrams. Explain the remedial measures.

(d) Draw and explain briefly the n-well CMOS design rules.

(e) Derive expressions for the drain-to-source current in the non-saturated and saturated regions of operation of an nMOS transistor.

(f) Define and derive the transconductance of nMOS transistor.

(g) Discuss small signal model of MOS transistor.

(h) Give a brief account of timing control and delay in Verilog.

Section-C

Attempt any two questions from this section. (15×2=30)

3. Draw the circuit for inverter using bipolar n MOS and CMOS technologies and compare them with respect to power consumption and speed.

4. Describe the principle of operation of barrel shifter. How can we build a circuit that can select an arbitrary n bit.

5. (a) What are goals and objectives of floor planning? Briefly discuss the three phases of floor planning.

(b) Define duty cycle, setup time, hold time.